# PATENT ABSTRACTS OF JAPAN

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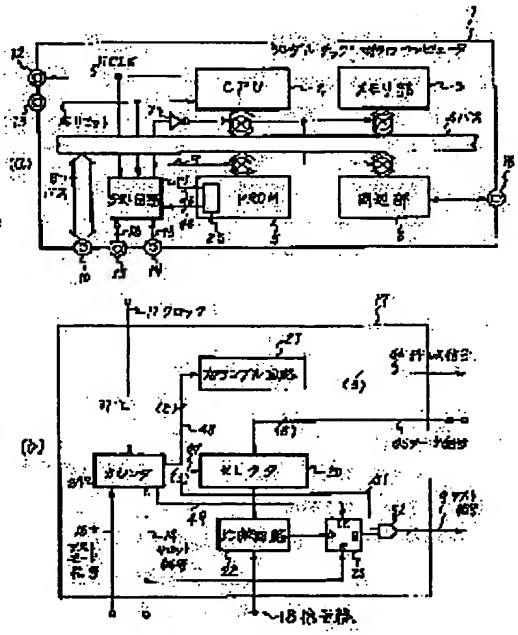
## (54) SINGLE CHIP MICROCOMPUTER

(57)Abstract:

PURPOSE: To protect data stored in a built-in ROM by enabling a test mode by inputting a password from the outside.

CONSTITUTION: A circuit to enable the test mode is composed of a scramble circuit 21, a comparator circuit 22, a counter 24 and a selector 20, the password is serially inputted from the outside by a signal 18 and data are read from a built-in ROM 5 with the output of the scramble circuit 21 as an address, and compared through the selector 20 for each unit of one bit. The counter 24 counts the number of times of comparing data and, when it reaches the prescribed number of times, the comparison is stopped. The comparator circuit 22 compares the stored data of a PROM with the input password from the outside, a signal 9 is outputted only when they are coincident with each other, and the test mode is enabled. Therefore, high-secrecy data stored in the built-in ROM are hardly accessed, and the danger of malicious use is reduced as well.



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## CLAIMS

[Claim(s)]
[Claim 1] In the single chip microcomputer which accumulated a central processing unit, the storage section, the periphery, and the programmable ROM (it is called Following PROM) on the single semi-conductor substrate, and contained the test facility to this PROM The scramble circuit which replaces the output address of the counter which carries out counting of the clock, and this counter, reverses, and is outputted as an address signal at the time of a test, The selector which chooses the data of said PROM corresponding to said address signal with the output of said counter, The test circuit which consists of comparator circuits which compare the data value inputted from the output and the outside of this selector is added. The single chip microcomputer characterized by enabling access to said PROM from the outside only when the value inputted from the outside and the storing value of said PROM are equal.
[Claim 2] The single chip microcomputer according to claim 1 whose test circuit is what performs addressing to the storing value of PROM with the data stored in this PROM.

[Translation done.]

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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the single chip microcomputer whose test was enabled, only when the data corresponding to the value stored especially in the built-in PROM are inputted from the outside about the single chip microcomputer which accumulated a memory function and computer ability on the single semi-conductor substrate.
[0002]
[Description of the Prior Art] In recent years, also in the field of a single chip microcomputer (henceforth a single chip microcomputer), high integration progresses by the advance of an LSI manufacturing technology, and the fall of the cost per unit function is also becoming remarkable.
[0003] Although the magnetic card has mainly been conventionally used in financial institutions, such as a bank, a magnetic card has little memory capacity, and has a problem in respect of security, and recently, many crimes, such as an unauthorized use and forgery, occur frequently, and it serves as a big social problem. Then, as what is replaced with this magnetic card, the IC card carrying a single chip microcomputer appears, and the large-scale experiment is progressing towards utilization in in and outside the country. Compared with a magnetic card, the storage capacity of this IC card is also large several steps, and since it contains computer ability in a card, it has marked reliability also in respect of security.
[0004] In the IC card which generally carried the single chip microcomputer, UVEPROM (Ultra-Violet

ErasableProgrammable ROM) or EEPROM (Electrical Erasable Programmable ROM) was used for the great portion of data memory (Following UVEPROM and EEPROM is called PROM), the data memory was divided into some fields, and the access is managed.

[0005] When using an IC card as the ATM card which financial institutions, such as a bank, publish, and a credit card, a part of this divided data memory is used for storing the high data of confidentiality, such as a secret zone (Secret Zone), a call, the account number of a bank, ID number, and a secret number. At the time of use, it is a part important when preventing the unauthorized use of an IC card, and forgery, this secret zone manages access to that field with software, and only when special, it can access to said field. However, at the time of a static test mode, direct access was easily more possible than the exterior to all the fields of Built-in PROM, and it was possible to have read and abused the value in a secret zone, or to have changed it intentionally.

[0006] Drawing 6 is the block diagram of an example of this kind of single chip microcomputer. In drawing 6 , the read-only or memory which uses the memory section 3 for user program storing and storing of data and in which a read-out store is possible, the bus by which an internal bus 4 transmits the address and data to time sharing, and an internal bus 8 are time-sharing buses used in case the address and data are transmitted to an internal bus 4 through the external terminal 10 at the time of a static test mode.

[0007] A central processing unit (it is called Following CPU) 2 performs data processing according to the program stored in the memory section 3. A periphery 6 consists of ports for performing the communication link with the chip exterior etc., outputs the data inputted through the internal bus 4 to the external terminal 26, inputs data from the external terminal 26, and has the function outputted to an internal bus 4. PROM5 consists of UVEPROM and an EEPROM as data memory, forms the secret zone 25 in memory, stores ID number of a card, a secret number, the account number, etc., and performs read-out and writing with the instruction of CPU. The user is performing the access control to this secret zone 25 with software. .

[0008] A terminal 15 is an external input terminal set to "1" at the time of a static test mode, since the output of an inverter 7 is set to 0 at this time, only PROM 5 is connected to an internal bus 4, and access to PROM5 becomes directly possible from the chip exterior. It connects with an internal bus 4, and the terminal which outputs the CPU clock 11 with which CPU2 outputs a terminal 12, and a terminal 13 are terminals which reset CPU2, at the time of "1", a terminal 10 is a terminal which outputs and inputs the address and data outside through an internal bus 8, and it resets [ a reset signal 14 is set to "1" and ] CPU2.

[0009] Next, the actuation at the time of a test is explained. A terminal 15 is set to "1" for a terminal 13 with "1", and a terminal 13 is set to 0 synchronizing with falling of the CPU clock 11. At this time, since a test signal 9 is set to "1" and the output of an inverter 7 is set to "0", CPU2, the memory section 3, and a periphery 6 are electrically separated from an internal bus 4. Therefore, connecting with an internal bus 4 is set only to PROM5. The address and data are inputted into PROM5 through the external terminal 10 and an internal bus 8 in this condition, and read-out and the writing of data are performed. At this time, if the address of the secret zone 25 is inputted, it is easily accessible to the data in a zone. Therefore, a data lead and a light can be performed easily.

[0010] As stated above, in the conventional single chip microcomputer, a user's software is performing all the access controls to the secret zone which stores secrecy data. When such a single chip microcomputer is carried in a card, it is possible by using a static test mode to perform an unjust data access to a secret zone. Since the electrical potential difference for writing will be automatically generated inside PROM if a write instruction is executed when the electric elimination mold read-only memory (EEPROM) is furthermore used for data memory, unjust writing is able to carry out easily to a secret zone.

[0011]

[Problem(s) to be Solved by the Invention] As mentioned above, since software is performing all the access controls to Built-in PROM in the single chip microcomputer which has managed access to the secret zone which is the field of access protection, in the conventional data memory, it is easily accessible at the time of a static test mode, and the fault that the data in a secret zone were abused and there was a danger that unjust access will be performed and data will be rewritten intentionally existed.

[0012] By adding an easy test circuit, the purpose of this invention eliminates unjust access at the time of a static test mode, and more positive security is to offer the single chip microcomputer obtained easily.

[0013]

[Means for Solving the Problem] In the single chip microcomputer which the configuration of this invention accumulated a central processing unit, the storage section, the periphery, and the programmable ROM (it is called Following PROM) on the single semi-conductor substrate, and contained the test facility to this PROM The scramble circuit which replaces the output address of the counter which carries out counting of the clock, and

this counter, reverses, and is outputted as an address signal at the time of a test, The selector which chooses the data of said PROM corresponding to said address signal with the output of said counter, The test circuit which consists of comparator circuits which compare the data value inputted from the output and the outside of this selector is added, and only when the value inputted from the outside and the storing value of said PROM are equal, it is characterized by enabling access to said PROM from the outside.

[0014]

[Example] Drawing 1 (a) and (b) are the block diagram of the single chip microcomputer of the 1st example of this invention, and the block diagram of the test circuit 17. In this example, components other than test circuit 17 newly added do not have the conventional example of drawing 6 , and a difference. Therefore, it explains centering on a test circuit 17.

[0015] In drawing, a test circuit 17 has the function to permit a static test mode, only when the bit-serial data value which inputted data into the serial and was inputted from the value stored in the secret zone 25 in PROM5 and the exterior is compared and it is in agreement from the external terminal 19 synchronizing with the clock signal 11 which CPU outputs.

[0016] The test circuit 17 of this example consists of a latch circuit 23, the scramble circuit 21, a comparator circuit 22, a counter 24, and the 2 input AND gate 52 like drawing 1 (b). The scramble circuit 21 scrambles the PROM address 48 which a counter 24 outputs, and outputs an address signal 46 to PROM5. According to the select signal 47 which a counter 24 outputs, a selector 20 selects 1 bit from input data, and outputs it to a comparator circuit 22. When in agreement and not in agreement [ a comparator circuit 22 compares the input data 18 from the outside with the output of a selector 20, and ] in "1", it outputs "0" to a latch circuit 23.

[0017] A counter 24 loads count data synchronizing with falling of a reset signal 14, and synchronizes with the standup of the basic clock 11, the static test mode signal 16 is "1", and only when a reset signal 14 is "0", it carries out the down count of the CPU clock 11. A latch circuit 23 latches the output of a comparator circuit 22 by the falling synchronization of the count signal 49 which a counter 24 outputs, and outputs it to the AND gate 52. Moreover, it is cleared by "0" when a reset signal 14 is "1." When a reset signal 14 is "0", a latch circuit 23 holds "0" until a reset signal 14 will be henceforth set to "1" again in "1", if "0" is latched after a latch. The AND gate 52 considers as an input the control signal 51 which the output of a latch circuit 23 and a counter 24 output, and outputs an AND output as a test signal 9.

[0018] Hereafter, actuation of a test circuit 17 is explained using the timing chart of drawing 2 . First, the static test mode signal 16 is set to "0" for the reset signal 14 with "1." Next, test signal mode 16 is set to "1", and a reset signal 14 is set to "0" synchronizing with falling of the CPU clock 11. At this time, a latch circuit 23 is cleared in falling of a reset signal 14. Moreover, a counter 24 loads initial value to a built-in down counter and a latch. Hereafter, "7" and the load value to a latch are explained for loading to a down counter as "3."

[0019] Synchronizing with the standup of the CPU clock 11, 8 bit data are inputted into a serial from the external terminal 19. At this time, a counter 24 is counted 8 times synchronizing with the standup of the CPU clock 11. Furthermore, the storing value to the down counter of a counter 24 and latch's storing value are respectively outputted as the select signal 47 of a triplet, and the PROM address of a triplet. The PROM address 48 of a triplet is scrambled (exchange reversal of an address signal etc.), and the scramble circuit 21 outputs it to PROM5 as an address signal 46 of a triplet. After 8 times count actuation, the down counter in a counter 24 sets a control signal 51 to "1", and stops.

[0020] A comparator circuit 22 outputs "1" to a latch circuit 23, when the value of the signal 18 inputted from the value which a selector 20 outputs, and the outside is the same. Moreover, "0" is outputted when not the same. A selector 20 chooses and outputs 1 bit specified with the select signal 47 which a counter 24 outputs to the data signal 45 which is storing data of PROM5 which carried out the address by the address signal 46.

[0021] Therefore, in the test circuit 17 of this example, a result is latched for the signal 18 which is input data from 1 bit and the outside of a data signal 45 which is data in PROM5 chosen with the select signal 47 outputted while a counter 24 carries out a down count to a latch circuit 23 as compared with bitwise. And only the number of bits (here 8) specified with the load value to a down counter is compared, and only when all bits are in agreement, the final value of a latch circuit 23 is set to "1." Moreover, since a counter 24 outputs "1" to a control signal 51 after ending a down count, the AND gate 52 outputs "1" to a test signal 9, and it permits a static test mode.

[0022] the case where this comparison is not in agreement at least 1 bit — the final value of a latch circuit 23 — 0 — becoming — a test signal 9 — "0" — therefore, a static test mode is forbidden. Therefore, since a static test mode is permitted only when in agreement with the data which entered from the outside the password of the

bit specified with the load value +1 to the down counter in a counter 24, and were built in PROM5, it is difficult to realize a static test mode unjustly compared with the former. Furthermore, since the bit size of a password and the address [ as opposed to / are adjustable and / the password storing value in PROM ] are scrambled, unjust access to the built-in PROM by the static test mode becomes increasingly difficult.

[0023] Drawing 3 is the block diagram showing the configuration of the counter 24 of drawing 1 . This counter 24 consists of a down counter 41 of 43 or 4 bits of constant generating circuits, the AND gate 44, and triplet latch 42. When a reset signal 14 is "1", the down counter 41 is cleared, actuation is suspended and latch 42 is also cleared. If a reset signal 14 is set to "0", the output of the constant generating circuit 43 is loaded to the low order triplet of latch 42 and the down counter 41 by falling synchronization. Moreover, since the static test mode signal 16 is "1", the down counter 41 is counted down synchronizing with the standup of the output of the AND gate 44, and outputs latch's 42 storing value as the PROM address 47. Moreover, the down counter 41 outputs the contents of the low order triplet of a counter as a select signal 48, carrying out a down count, and outputs the clock of a counter of operation as a count signal 49.

[0024] Hereafter, the load value to the down counter 41 is explained as 7. if the down counter 41 carries out a down count 8 times — the 1- since the 4th bit is set to "1", the output of the AND gate 44 is also set to "0", and the down counter 41 suspends count actuation. At this time, a select signal 48 is outputted eight patterns to 7-0. Therefore, a select signal 48 is outputted corresponding to all the bits of a data signal 45.

[0025] In this example, by adding the test circuit 17 which consists of easy hardware, implementation of the static test mode by the third person becomes less easy, unjust access to the data in the secret zone 25 and disappearance of data can be prevented, and advanced fail-safe is realized.

[0026] Drawing 4 and drawing 5 are the block diagram of the test circuit of the single chip microcomputer of the 2nd example in this invention, and the block diagram of the counter of drawing 4 . The block diagram of drawing 4 is different only in that the pass from PROM5 to counter 24a is prepared to drawing 1 . Therefore, only the configuration and actuation of counter 24a are described.

[0027] Counter 24a of the single chip microcomputer of this example is different to the counter 24 of drawing 1 in that the value built in PROM5 in the down counter 41 and the latch 42 is specified as an initial load value.

[0028] This counter 24a performs down count actuation after loading initial value to latch 42 and the down counter 41 from PROM25 corresponding to the scramble value of the address "0." Namely, when a reset signal 14 is changed from a high to a low instead of the load value which the constant generating circuit 43 generates unlike the 1st example, latch's 42 cleared storing value "0" is addressed by the address signal 46 after a scramble in the scramble circuit 21, and it latches to latch 42 in falling of a reset signal 14 by making into a load value the data signal 45 led from PROM5. Therefore, by changing the value stored in the address which scrambled - address "0", since the storing address of a password can be changed, it is effective in security becoming high more to the 1st example.

[0029] Test circuit 17a outputs a test signal 9, only when the storing data of PROM5 and the input data from the outside which were specified by the latch 42 are in agreement, and it realizes a static test mode. The actuation after loading initial value to latch 42 and the down counter 41 is the same as that of the 1st example.

[0030]

[Effect of the Invention] The unjust data access produced while performing the data access to a secret zone freely by implementation of a static test mode conventionally by adding the test circuit which permits a static test mode, only when the data stored in Built-in PROM and the data inputted from the exterior are in agreement in this invention, as explained above is forbidden, and it is effective in realizing advanced security.

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## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] (a) and (b) are a single chip microcomputer in the 1st example of this invention, and the block diagram of the test circuit.

[Drawing 2] The timing chart explaining actuation of the test circuit of drawing 1 .

[Drawing 3] The block diagram of the counter in a test circuit of the example of drawing 1 .

[Drawing 4] The block diagram of the test circuit in the 2nd example of this invention.

[Drawing 5] The block diagram of the counter in the test circuit of drawing 4 .

[Drawing 6] The block diagram of an example of the conventional single chip microcomputer.

[Description of Notations]

1 1a Single chip microcomputer
2 CPU
3 Memory Section
4 Eight Internal bus
5 PROM
6 Periphery
7 Inverter
9 Test Signal
10–13, 15, 19, 26 External terminal
11 CPU Clock
14 Reset Signal
16 Static Test Mode Signal
17 17a Test circuit
18 Signal Line
20 Selector
21 Scramble Circuit
22 Comparator Circuit
23 Latch Circuit
24 24a Counter
25 Secret Zone
41 Down Counter
42 Latch
43 Constant Generating Circuit
44 52 AND gate
45 Data Signal
46 Address Signal
47 Select Signal
48 PROM Address
49 Count Signal
51 Control Signal

[Translation done.]